Exhibit J

No. 21-1772

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

ACQIS, LLC,

Plaintiff-Appellant,

v.

EMC CORPORATION,

Defendant-Appellee.

Appeal From The United States District Court For The District Of Massachusetts
No. 1:14-cv-13560-ADB, District Judge Allison Dale Burroughs

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REPRESENTATIVE CLAIMS

U.S. Patent No. 8,041,873 (Claim Nos. 29 and 61)[1]

29. A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a connector, and

a first pair of unidirectional, multiple bit, low voltage differential signal (LVDS) channels to transmit encoded ***Peripheral Component Interconnect (PCI) bus transaction*** as serial data along a pair of directions that are different from each other; and

a computer module coupled to one of the coupling sites through the connector of the one of the coupling sites, the computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a mass storage device coupled to the processing unit,

a second pair of unidirectional, multiple bit, LVDS channels to transmit encoded PCI bus transaction as serial data along a pair of directions that are different from each other, and

an interface controller coupled to the second pair of LVDS channels,

wherein the interface controller is coupled to the console for data communication upon coupling of the computer module to the console.

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[1] Emphasis added to limitations at issue.

[54.[2] A computer module insertable into a coupling site of a console for data communication, comprising:

a main circuit board;

a processing unit coupled to the main circuit board;

a main memory coupled to the processing unit;

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions for ***communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction***; and

a peripheral bridge directly coupled to the processing unit, the peripheral bridge comprising an interface controller directly coupled to the LVDS channel.]

61. The computer module of claim 54, wherein the encoded serial bit stream of PCI bus transaction comprises encoded ***PCI address and data bits.***

[2] Asserted claim 61 depends from claim 54, but claim 54 itself is not asserted.

CERTIFICATE OF INTEREST

Counsel for Defendant-Appellee EMC Corporation certifies the following:

1. The full name of every entity represented by me is:

   EMC Corporation

2. The parties named in the caption are the real parties in interest.

3. All parent corporations and any publicly held companies that own 10 percent or more of the stock of Appellee are as follows:

   Dell Inc., which is wholly owned by Denali Intermediate Inc., which is wholly owned by Dell Technologies Inc., a publicly traded company. No other publicly held corporation owns 10% or more of the stock of EMC Corporation.

4. The names of all law firms and the partners or associates that appeared for Appellee in the trial court or are expected to appear in this court (and who have not or will not enter an appearance in this case) are:

   GIBSON, DUNN & CRUTCHER LLP: Matthew D. McGill, Laura Corbin

   Formerly of GIBSON, DUNN & CRUTCHER: Blair A. Silver, Jessica L. Greenbaum, Jordan H. Bekier, Nicholas R. Fung

   HINCKLEY ALLEN & SNYDER: Christine K. Bush, Laurel M. Gilbert, Michael J. Connolly

   EMC CORPORATION: Krishnendu Gupta

5. There are no other pending cases that may affect or be affected by this appeal.

6. There are no organizational victims or bankruptcy case debtors or trustees in this appeal.

Dated: November 19, 2021

/s/ Mark A. Perry

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STATEMENT OF RELATED CASES

Pursuant to Federal Circuit Rule 47.5, Appellee EMC Corporation identifies the following related cases:

- *ACQIS LLC v. Samsung Elecs. Co., et al*., No. 2:20-cv-00295 (E.D. Tex.);
- *ACQIS LLC v. Acer Inc.,* No. 2:21-cv-00275 (E.D. Tex.);
- *ACQIS LLC v. MITAC Holdings Corp., et al*., No. 6:20-cv-00962 (W.D. Tex.);
- *ACQIS LLC v. Inventec Corp*., No. 6:20-cv-00965 (W.D. Tex.);
- *ACQIS LLC v. Asustek Comput., Inc*., No. 6:20-cv-00966 (W.D. Tex.);
- *ACQIS LLC v. Lenovo Grp. Ltd., et al*., No. 6:20-cv-00967 (W.D. Tex.);
- *ACQIS LLC v. Wistron Corp., et al*., No. 6:20-cv-00968 (W.D. Tex.).

INTRODUCTION

The judgment should be affirmed for two independent reasons:

First, the asserted claims are limited to a "PCI bus transaction," which the district court correctly construed to mean compliance with the "*entirety*" of the PCI Local Bus Specification, including "*all information* required by the PCI standard." Appx0008–0009, Appx0012–0013 (emphasis added). It is undisputed that the accused products do not comply with the PCI standard or generate all of the information it requires. *See* Appx2235–2359. On appeal, ACQIS continues to argue that the limitation includes only *some* of the information required by the PCI standard, but this position is refuted by the intrinsic evidence.

Second, even if ACQIS's proposed construction of the term "PCI bus transaction" were correct, the district court also construed the claims to require parallel-to-serial conversion of the information comprising such a transaction. Appx0012. On appeal, ACQIS has not challenged the district court's finding that the accused products do not infringe under that construction. Instead, ACQIS continues to argue that the claims do not require parallel-to-serial conversion of a PCI bus transaction. This position cannot be reconciled with the intrinsic evidence, and is contradicted by ACQIS's submissions to the Patent Trial and Appeal Board.

Because the accused devices do not practice either or both of these limitations, the district court properly granted summary judgment of non-infringement.

STATEMENT OF THE ISSUES

Whether the district court correctly granted summary judgment of non-infringement because:

1. The "PCI bus transaction" limitation requires compliance with the entirety of the PCI Local Bus Specification, including all information required by the PCI standard; and/or

2. The asserted claims require parallel-to-serial conversion of the information that comprises a PCI bus transaction.

STATEMENT OF THE CASE

I. Background

The asserted patents disclose a transaction compliant with the then-prevailing PCI standard, communicated using a serial interface instead of the prior-art parallel connection. By contrast, the accused products do not generate or communicate all information required by the PCI standard, nor do they convert the information comprising a parallel PCI bus transaction to serial form.

A. The Prior Art: Parallel Communications Using A PCI Bus

At the time the earliest applications leading to the asserted patents were filed, most computers relied on a well-known and predominant standard interface called Peripheral Component Interconnect, or PCI. This interface sent multiple bits of information simultaneously over multiple wires (i.e., in parallel), known as a PCI bus. One common use of such a PCI bus was to interconnect two PCI-compliant

devices, such as a computer and a peripheral. The inventors of the asserted patents do not claim to have invented PCI. To the contrary, the purported invention utilizes the PCI bus that was already ubiquitous in computing devices in a purportedly novel way.

Data communications that can be transmitted across a PCI bus (referred to as "PCI bus transactions") are defined by the PCI Local Bus Specification, which sets out in exacting detail the requirements of the PCI standard. Appx2235–2359 (excerpts). As ACQIS concedes (Br. 45 & n.5), the PCI Local Bus Specification is intrinsic evidence because it is cited on the face of the asserted patents. This PCI standard defines a transaction to be an exchange of information that takes place in a specific sequence and manner. For example, the PCI Local Bus Specification specifies both the information that must be communicated and how it is transmitted. Appx2244; Appx2246; *see also* Appx1271, ¶ 62.

The PCI Local Bus Specification defines other requirements for a PCI bus transaction. A PCI bus transaction occurs in two "phases," i.e., periods of time in which certain signals and information are sent—"an address phase followed by one or more data phases." Appx2246 (footnote omitted); *see also* Appx2358. During each phase, 32 bits (representing either address or data signals) are generated for parallel transmission. Appx2246. These signals are abbreviated as "AD" in the PCI

Local Bus Specification, and are sent on "AD[31::00]" pins (or lines) (each pin carries one bit of AD information). *See id.*

In addition to the AD signals, the PCI Local Bus Specification also requires a PCI bus transaction to include signals known as control, command and byte enable, and parity. Control signals control the timing of data exchange (i.e., define the beginning and end of the various phases of the PCI bus transaction). For example, the PCI Local Bus Specification explains that "FRAME#," "IRDY#," "TRDY#," and "DEVSEL#" signals delineate a PCI bus transaction: "The address phase is the clock cycle in which FRAME# is asserted" and that "[d]ata is transferred during those clocks where both IRDY# and TRDY# are asserted." Appx2246; *see also* Appx2273–2274 (explaining that a read or write transaction "starts . . . when FRAME# is asserted for the first time"). The PCI Local Bus Specification explains that control signals are "fundamental[]" to "all PCI data transfers":

3.2.1. Basic Transfer Control

The fundamentals of all PCI data transfers are controlled with three signals (see Figure 3-1).

FRAME#	is driven by the master to indicate the beginning and end of a transaction.
IRDY#	is driven by the master to indicate that it is ready to transfer data.
TRDY#	is driven by the target to indicate that it is ready to transfer data.

Appx2262.

Command and byte enable signals (abbreviated as "C/BE" in the PCI Local Bus Specification) are signals that inform each PCI-compliant device of the type of transaction that is occurring (e.g., a read or write). Appx2246; Appx2258–2260; *see also* Appx2355–2356 (defining "bus commands" and "command"). C/BE signals are sent on the "C/BE[3::0]#" pins. Appx2246.

The PCI Local Bus Specification clearly and consistently distinguishes between control and command/byte enable signals, which must be sent on separate pins. *See* Appx2246–2247 (describing "C/BE[3::0]#" pins that carry "Bus Command and Byte Enable[]" signals as part of the "Address and Data Pins" functional group and distinct from the separate "Interface Control Pins" functional group); Appx2258–2262 (discussing command signals in a separate section (3.1) from control signals (3.2)).

A one-bit parity signal (abbreviated as "PAR" in the PCI Local Bus Specification) used for error detection is also required in a PCI bus transaction. "***Parity generation is not optional***; it must be done by all PCI compliant devices." Appx2332 (emphasis added); *see also* Appx2247 ("Parity generation is required by all PCI agents"). Parity is generated from the AD and C/BE signals, and is categorized as part of the "Address and Data Pins" functional group. Appx2246–2247; *see also* Appx2244 (annotated in red):

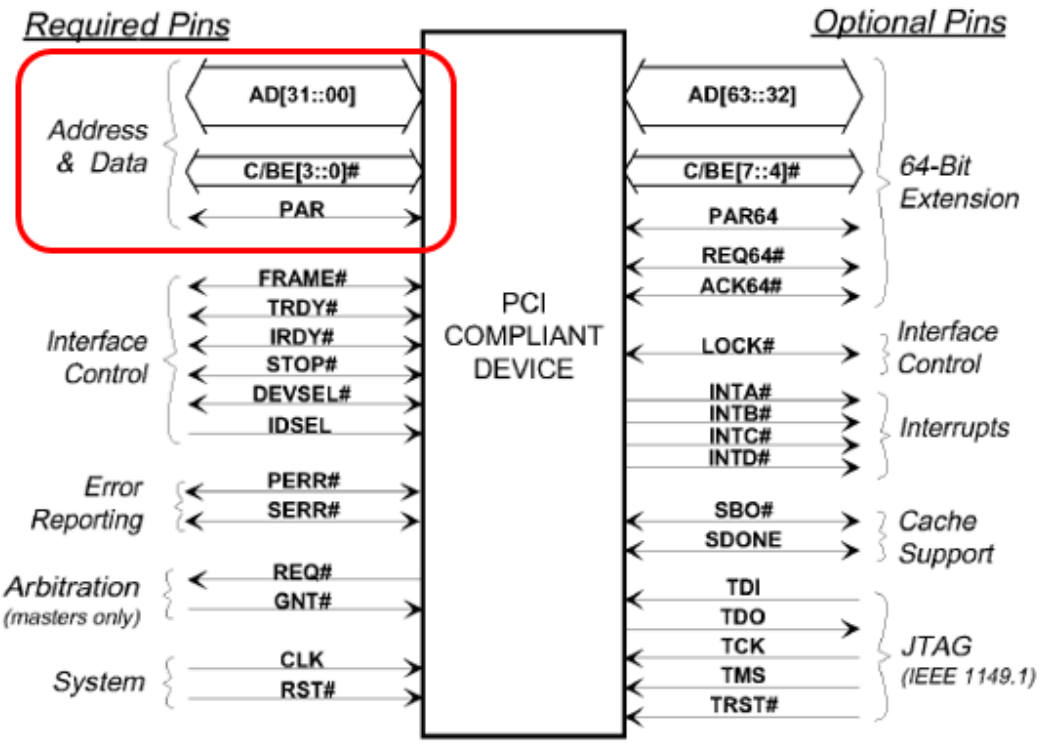

Figure 2-1: PCI Pin List

A parity signal is sent after each phase of the PCI bus transaction (i.e., after the address phase and again after each data phase) "and lags the corresponding address or data by one clock." Appx2332; Appx2247; *see also* Appx2333:

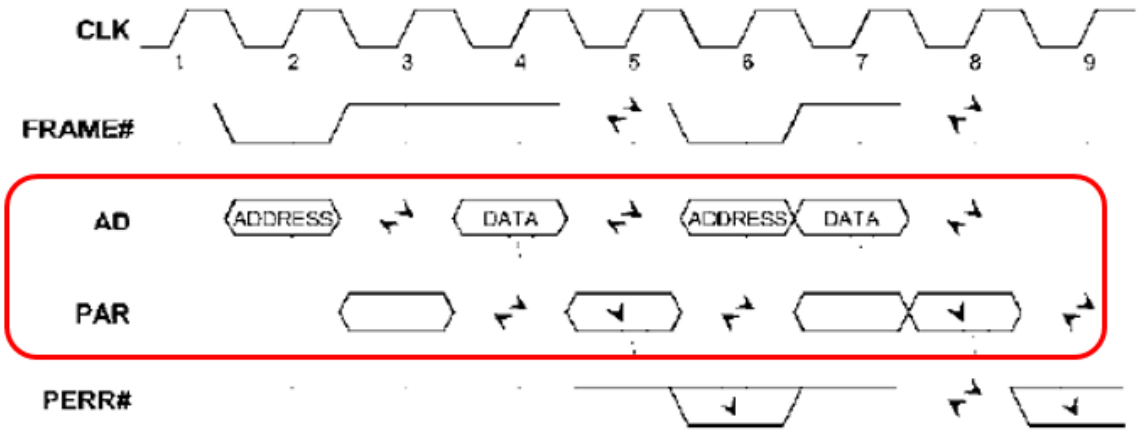

Figure 3-26: Parity Operation

Thus, in addition to including command, address, and data signals, the PCI Local Bus Specification requires a PCI bus transaction to necessarily also include at least control and parity signals and to be transmitted in specific phases. It is undisputed that the accused products do not include these signals. Appx0008.

B. The Asserted Patents: A New Serial Interface Using The PCI Standard

ACQIS asserts eleven claims from eight patents in this litigation. These patents descend from related applications filed by the same inventor, and describe virtually identical subject matter.[3]

The asserted patents sought to speed up computer communications by replacing the prior art parallel connections between PCI-compliant devices with a faster serial interface. *See* Appx0782 ("[O]ne key to the invention was to serialize the otherwise parallel PCI bus transactions to increase communication speeds for peripherals"). Due to the predominance of the PCI standard, the claimed inventions needed to be "completely compatible with existing peripheral devices." *Id.*

[3] ACQIS asserted claim 60 of U.S. Patent No. 7,363,416 ("the '416 patent"); claims 38 and 49 of U.S. Patent No. 7,818,487 ("the '487 patent"); claims 9, 29, and 61 of U.S. Patent No. 8,041,873 ("the '873 patent"); claim 44 of U.S. Patent No. RE41,294 ("the '294 patent"); claim 31 of U.S. Patent No. RE42,814 ("the '814 patent"); claim 39 of U.S. Patent No. RE43,119 ("the '119 patent"); claim 24 of U.S. Patent No. RE43,171 ("the '171 patent"); and claim 29 of U.S. Patent No. RE44,468 ("the '468 patent"). Because the asserted patents contain similar specifications, EMC cites to the '873 patent unless otherwise specified.

Thus, the claimed invention did not purport to modify the internal parallel PCI buses already present in computers and peripherals. The asserted patents still require complete PCI bus transactions on either side of the claimed serial channel, including all address and data, command and byte enable, control, and parity signals. *See* Appx0782 ("The claims reflect this invention with their focus on the serialized PCI bus transaction"). For example, the '873 patent family explains that "bits transmitted on lines PD0 to PD3" of the new serial interface "represent 32 PCI AD[31::0] signals, 4 PCI C/BE# [3::0] signals, and . . . ***PCI control signals, such as FRAME#, IRDY#, and TRDY#***." Appx0153 ('873 patent, 20:44–47) (emphasis added); *see also, e.g.*, Appx0045 ('416 patent, 20:61–64) (same); Appx0094 ('487 patent, 20:39–42) (same). All asserted patents also describe a "transmitter" that "receives multiplexed parallel address/data (AID) bits ***and control bits***" sent "on the AD[31::0] out and ***the CNTL out lines, respectively***." Appx0152 ('873 patent, 17:41–43) (emphasis added); *see also, e.g.*, Appx0192 ('294 patent, 13:30–32); Appx0330 ('171 patent, 16:1–3). Thus, even without a physical PCI bus connecting two peripheral devices, the claimed inventions nonetheless generate all of the information defined in the PCI Local Bus Specification to maintain compatibility with the PCI standard.

Just like the PCI Local Bus Specification, the asserted patents also clearly distinguish control signals (e.g., FRAME#) from command signals (e.g., read/write

commands). Both types of signals must be included in a PCI bus transaction.[4] Indeed, the asserted patents expressly define "control signals" with reference to the PCI standard. *See, e.g.*, Appx0152 ('873 patent, 17:28–32) ("Examples of control signals include ***PCI control signals*** and CPU control signals. ***A specific example of a control signal is FRAME# used in PCI buses. A control bit . . . is a data bit that represents a control signal***." (emphasis added)); Appx0192 ('294 patent, 13:16–20); Appx0330 ('171 patent, 15:55–58). The '873 patent family also describes that in Figure 13, "***CM0# to CM3# represent 4 bits of PCI command information*** . . . and ***CN0 to CN9 represent 10 bits of control information*** sent in each clock cycle." Appx0153 ('873 patent, 20:30–37) (emphasis added)); *see also, e.g.*, *id.* ('873 patent, 20:44–47) ("The bits transmitted on lines PD0 to PD3 represent 32 PCI AD[31::0] signals, ***4 PCI C/BE# [3::0] signals***, ***and*** . . . ***PCI control signals, such as FRAME#, IRDY#, and TRDY#***" (emphasis added)).

C. PCI Express: A New, Distinct Protocol That Replaced The PCI Standard

By the mid- to late-1990s, as computer components became more powerful, the industry noticed some disadvantages of the PCI standard, including its limited bandwidth and transmission speeds. An effort was undertaken to develop a

[4] Because there are no material differences pertinent to this appeal between command and byte enable signals, EMC henceforth refers to both collectively as "command signals."

replacement, which led to the creation "from the ground up" of a new standard. Appx3289. Initially called "3GIO" (for "Third Generation I/O"), this new standard was later renamed to "PCI Express" "solely for purposes of branding and for maintaining consistency in the marketplace." Appx3295. Ajay Bhatt, the creator and lead architect of this standard, explained that "[t]he name 'PCI Express' was not meant to indicate any hardware or protocol compatibility with the PCI Local Bus Specification." *Id.*

Unlike the PCI standard, which was built on a parallel bus architecture, Mr. Bhatt explained that PCI Express was "a new, fully serial, point-to-point interconnect." Appx3296; *see also* Appx2364–2365. PCI Express was never designed to be "a serialized version of the PCI Local Bus or a serialization of a PCI bus transaction in accordance with the PCI Local Bus Specification," Appx3296, and "does not require converting a conventional PCI bus transaction from parallel to serial," Appx3310. Indeed, unlike the claimed invention, "PCI Express is not compatible with the PCI Local Bus Specification transaction protocol" and "does not generate, encode, or communicate PCI bus transactions in accordance with the PCI Local Bus Specification." Appx3309–3310.

Mr. Bhatt identified specific examples of how the two standards differ. He testified that "PCI Express does not execute transactions in 'phases,' as described in the PCI Local Bus Specification," but is instead "a packet-based protocol, using

'Transaction Layer Packets' (TLPs) to communicate." Appx3310. He also explained that PCI Express "does not need or use any of [FRAME#, IRDY#, and TRDY#] control signals," Appx3315–3316; *see also* Appx2366, and "does not transmit a parity bit" for error correction, as required by the PCI Local Bus Specification, instead relying on "a Cyclic Redundancy Check (CRC) and Error Correcting Code (ECC)," Appx3318.

In other words, Mr. Bhatt did not create PCI Express to be the next version of PCI. He created a brand new protocol that is fundamentally different and incompatible with the PCI standard claimed in the asserted patents.

II. Claim Construction Proceedings

ACQIS sued EMC in the Eastern District of Texas on September 9, 2013, Appx0002, where Judge Davis issued a claim construction opinion on April 13, 2015, Appx0498–0529. The case was then transferred to the District of Massachusetts and assigned to Judge Burroughs. Shortly thereafter, the litigation was stayed pending two *inter partes* review ("IPR") petitions filed by EMC challenging several claims of the '873 and '814 patents. Appx0531; Appx0599. After the IPR proceedings concluded and the stay of litigation was lifted, EMC moved to revisit claim construction based on ACQIS's statements made in the IPRs. EMC explained that it was fundamentally unfair for ACQIS "to define its claims one way (i.e., narrowly) in the IPRs to avoid invalidity and a totally different way (i.e.,

broadly) in this Court to prove infringement." Appx1118. Judge Burroughs issued a second *Markman* order on December 8, 2017. Appx1695–1712.

The claim construction proceedings relevant to the terms at issue on appeal are summarized below.

A. "PCI Bus Transaction"

1. Before Judge Davis, both parties agreed that, consistent with the intrinsic record, the construction of "PCI bus transaction" requires compliance with the PCI standard. *See* Appx0390–0391; Appx0445; Appx0507. The parties disagreed only as to whether a "PCI bus transaction": (1) requires a physical PCI bus, and (2) is limited to command, address, and data information. ACQIS proposed to construe "PCI bus transaction" to mean "digital command, address, and data information, in accordance with the PCI standard, for communication with an interconnected peripheral component." Appx0505. EMC proposed that the term should be construed instead to mean "signals communicated over a PCI bus." *Id.*

Judge Davis agreed with ACQIS that no physical PCI bus was required. Appx0506–0507. Judge Davis, however, rejected the remainder of ACQIS's proposal because the PCI Local Bus Specification "does not clearly define a 'transaction' as digital command, address, and data information." Appx0507. Judge Davis concluded that "***a PCI bus transaction must include all information required***

by the PCI standard." *Id.* (emphasis added). ACQIS never sought reconsideration of this ruling.

2. Before the Board, both parties again agreed that a PCI bus transaction must be a "transaction" defined "according to [the PCI] protocol standard." Appx0675; *see also* Appx0679. Consistent with that understanding (and Judge Davis's construction), the Board construed "PCI bus transaction" to mean "PCI industry standard bus transaction," without any reference to command, address, or data information. Appx1071; Appx1096. Ultimately, the Board agreed with ACQIS that the prior art did not disclose a PCI bus transaction according to the "PCI industry standard." *See* Appx1100; Appx1076.

3. Before Judge Burroughs, EMC argued that ACQIS had conceded during the IPRs that a PCI bus transaction must be a "transaction" according to the PCI Local Bus Specification, not just any information. Appx1126. Consistent with this requirement, EMC also proposed that the related term "communicating . . . PCI bus transaction" (and similar terms) should be construed to mean "communicating a PCI bus transaction, including all address, data, and control bits, without discarding any of those bits." Appx1137. EMC explained that in the IPRs, ACQIS opposed EMC's position that the challenged claims did not require all bits to be communicated, and thus must be held to that disclaimer. Appx1138–1139.

In response, ACQIS formally agreed with Judge Davis's construction of "PCI bus transaction," arguing that "[n]othing warrants disturbing this construction." Appx1147; *see also* Appx1156 ("Both Judge Davis and the PTAB properly construed the term[] 'PCI bus transaction'"). ACQIS did not dispute that the asserted patents require a "transaction" in accordance with the PCI standard, instead challenging only EMC's argument that the asserted claims require a physical PCI bus. *See* Appx1162–1167; Appx1701.

ACQIS also argued that no construction was necessary for "communicating . . . PCI bus transaction" because the term carried plain and ordinary meaning. Appx1177–1178. ACQIS contended that EMC's proposed construction was supposedly inconsistent with claims that recite communicating only address and data bits (the so-called "address and data claims," such as, for example, claim 61 of the '873 patent). Appx1178. Although ACQIS disagreed that it made a "'clear and unmistakable' disavowal" in the IPRs, Appx1179, it acknowledged during the *Markman* hearing its IPR expert's agreement that control bits (which represent the PCI control signals) were a required part of a PCI bus transaction, Appx1641. ACQIS also agreed it would accept EMC's proposed construction if the last six words (i.e., "without discarding any of those bits") were omitted from that construction. Appx1643.

Judge Burroughs ruled that "the PCI Local Bus Specification does not define [a PCI bus transaction] by the presence of a PCI bus," but reiterated Judge Davis's conclusion that "a PCI bus transaction must include all information required by the PCI standard," and must "include the relevant industry standard, the PCI Local Bus Specification." Appx1701–1702. Judge Burroughs therefore left Judge Davis's construction in place, but changed the word "information" to "transaction" to reinforce the district court's ruling that "PCI bus transaction" must comply with all requirements of the PCI Local Bus Specification. Appx1704. Consistent with that ruling, Judge Burroughs construed "communicating . . . PCI bus transaction" to mean "communicating a PCI bus transaction, including all address, data, and control bits." Appx1711–1712.

B. "Encoded Serial Bit Stream Of Peripheral Component Interconnect (PCI) Bus Transaction" And Related Terms

The focus of the parties' dispute concerning this term was whether it required parallel-to-serial conversion of a PCI bus transaction. *See, e.g.*, Appx0507–0508; Appx1131–1134.

1. In Texas, focusing only on the word "encoded," ACQIS proposed that no construction was necessary for this term, or in the alternative, it should be construed to mean "assigning code to represent data for a bus transaction." Appx0396–0397. ACQIS argued that a PCI bus transaction need not originate in parallel form because several claims do not recite a physical PCI bus. Appx0397–0398; Appx0486.

In response, EMC pointed out that the term is not limited to the word "encoded," but should be read in context with the surrounding claim language and the specification, which require adherence to the PCI standard. *See* Appx0456. EMC explained that because a PCI bus transaction is inherently parallel due to the nature of the PCI standard, the claims require conversion from parallel to serial form. *See* Appx0456–0457. Accordingly, EMC proposed that the term should be construed to mean a "'PCI bus transaction' translated into bits for parallel to serial conversion." Appx0507.

Based on the evidence available at the time, Judge Davis disagreed that parallel-to-serial conversion was required, and construed this term to mean "code representing a PCI bus transaction." Appx0508.

2. The Board did not formally construe this term. Throughout the IPR proceedings, however, ACQIS repeatedly emphasized the importance to the asserted patents of converting parallel PCI bus transactions to serial form. *See, e.g.*, Appx0782; Appx0831; Appx1027; Appx1031. The Board also recognized this importance in its Final Written Decisions, explaining that the asserted patents "sought to overcome ***the disadvantages associated with using a parallel connector*** by encoding a PCI industry standard bus transaction ***so that it can be communicated on a serial connector***." Appx1074 (emphasis added); Appx1098–1099. The Board also noted that the claimed improvement of the asserted patents was to "interface[e]

two PCI buses"—which are indisputably parallel—"using a serial connector" and to encode a PCI bus transaction "so it can be communicated in serial form over" that serial connector. Appx1068; Appx1093.

3. In Massachusetts, EMC argued that Judge Davis's construction of this term should be revised based on ACQIS's repeated assertions during the IPRs that parallel-to-serial conversion is a critical aspect of the claimed inventions. EMC also explained that the claim language consistently requires "serializing" (i.e., converting) a PCI bus transaction from its original parallel form, because a PCI bus transaction is generated for use on a parallel PCI bus (whether one is required or not), and therefore must be serialized before transmission over a serial connector. Appx1131–1134. EMC pointed out that every embodiment disclosed in the asserted patents requires parallel-to-serial conversion. Appx1132.

In response, ACQIS argued that it did not make a clear and unmistakable disavowal during the IPRs to require parallel-to-serial conversion of a PCI bus transaction. Appx1147–1148; Appx1175–1177. ACQIS again focused solely on the term "encoded," arguing that the asserted patents disclose some "types of encoding . . . [that] do not require any form of parallel-to-serial conversion." Appx1174–1175.

Judge Burroughs rejected ACQIS's arguments, providing three and a half pages of quotations from the IPR proceedings, *see* Appx1705–1708, and concluding

that "***ACQIS's numerous and repetitive statements in the IPRs clearly and unmistakably show that an encoded PCI bus transaction requires that a PCI bus transaction be encoded for serial transmission from a parallel form***," Appx1708 (emphasis added). Judge Burroughs also explained that the claim language and asserted patents' specifications support requiring parallel-to-serial conversion, because the asserted patents claim the parallel PCI standard. *See* Appx1709. Judge Burroughs concluded that "[t]he claim language and specification, when read in context with the industry standard, support the construction that a PCI bus transaction is in a parallel form prior to being serialized," and construed this term to mean "a PCI bus transaction that has been serialized from a parallel form." Appx1709–1711.

III. Summary Judgment Of Non-Infringement

EMC moved for summary judgment on the ground that the accused products, which adhere to the PCI Express protocol that is entirely distinct from the PCI standard recited in the asserted patents, do not practice the "PCI bus transaction" limitation, nor do they convert a PCI bus transaction from parallel to serial form. Thus, under the district court's constructions, they do not infringe.

A. The Accused Products Do Not Generate Or Transmit A "PCI Bus Transaction"

EMC explained that EMC's accused products do not generate or communicate PCI bus transactions because the accused products: (1) do not generate or

communicate any of the control signals (or bits) defined in the PCI Local Bus Specification; (2) do not generate or communicate the required parity signals (or bits); and (3) do not use phases as required by the PCI Local Bus Specification. Appx1743–1748. ACQIS never alleged otherwise.

EMC also pointed out that even under ACQIS's improper and thrice-rejected construction of "PCI bus transaction," the accused products still do not infringe because they do not include a four-bit "command" signal as required by the PCI Local Bus Specification, but instead use a seven-bit code to represent packet types. Appx1753–1755; *see also* Appx2258 ("Command Definition" of the PCI Local Bus Specification listing the possible four-bit codes).

In response, ACQIS argued that none of the constructions by Judge Davis, the PTAB, and Judge Burroughs required a PCI bus transaction to include all of the signals specified by the PCI Local Bus Specification. Appx3341–3343. The crux of ACQIS's argument on summary judgment (as it is on appeal) was that because a physical PCI bus was not required by the construction of "PCI bus transaction," that limitation cannot include those signals that the PCI Local Bus Specification describes as related to the physical PCI bus. *See, e.g.*, Appx3333 (ACQIS arguing that control and parity signals are not part of a PCI bus transaction because "[t]hese features have no other use" than "to control a physical PCI Local Bus" (emphasis removed)); Appx3359–3360 (ACQIS arguing that a "four-bit command and byte

enable encoding format is not required absent a physical PCI Local Bus"); *see also* Appx3342–3343; Appx3349–3353; Appx3355–3356. On this basis, ACQIS also argued that by requiring communication of "control bits," the asserted patents must mean communicating "Bus Command and Byte Enable[]" bits, and attempted to rescind its agreement to the district court's construction of "communicating . . . PCI bus transaction." Appx3373–3376. ACQIS did not acknowledge that the PCI Local Bus Specification expressly requires control and parity signals, and a specific four-bit format for command and byte enable signals. Appx2258; Appx2332.

Judge Burroughs rejected all of ACQIS's arguments, explaining that they were nothing more than "***attempts to skirt the claim construction set forth by Judge Davis and this Court***." Appx0008 (emphasis added). Judge Burroughs pointed out that ACQIS has always agreed that a PCI bus transaction must be in accordance with the PCI Local Bus Specification, and that ***Judge Davis ruled that such a transaction*** "***must include all information required by the PCI standard***." Appx0008–0009 (emphasis added). The district court further explained that it "has already concluded that the claims are limited by the [PCI Local Bus] Specification ***in its entirety***." Appx0013 (emphasis added). Judge Burroughs also faulted ACQIS for raising untimely claim construction arguments, explaining that a district court is required to resolve only "fundamental disputes" about claim scope, and two district courts had already done so concerning this limitation. Appx0010. Judge Burroughs granted

summary judgment because "the accused products do not contain the limitations set forth in the asserted claims, which recite a PCI bus transaction with reference to the [PCI Local Bus] Specification." Appx0010–0011; *see also* Appx0013.

B. The Accused Products Do Not Serialize A Parallel PCI Bus Transaction

As an independent basis for non-infringement, EMC explained that the accused products do not convert a PCI bus transaction from parallel to serial form, as required by the district court's construction. EMC noted that ACQIS has never identified in the accused products a PCI bus transaction that is converted from parallel to serial form, or even a parallel transaction of any kind. Appx1758–1761.

EMC explained that the accused products convert from parallel to serial form only 10-bit symbols, each encoded from a single 8-bit byte of a PCI Express packet for easier transmission (what is known as "8b/10b encoding"). Appx1761 & n.24. EMC explained that this 8b/10b-encoded data cannot be a parallel "PCI bus transaction" because it does not include all of the signals and phases required by the PCI standard. Appx1761. EMC also explained that 8b/10b-encoded data in the accused products is not a PCI bus transaction *even under ACQIS's proposed construction*, because ACQIS conceded that a PCI bus transaction requires at least 32-bits of address or data sent in parallel, and a converted 10-bit block of data indisputably cannot convey 32 bits. Appx1761–1762.

In response, ACQIS again argued that control bits do not need to be included in a serialized PCI bus transaction because they are only used to control a physical PCI bus. Appx3365–3366. ACQIS also argued that a PCI bus transaction need not be converted from parallel to serial all at once, and thus converting 8b/10b-encoded data meets this claim limitation. Appx3370–3372.

Judge Burroughs rejected these arguments, noting that "ACQIS does not dispute that '[t]he asserted claims require a PCI bus transaction, beginning in parallel form, to be converted into serial form for transmission across a serial interface.'" Appx0012 (quoting Appx1781, ¶ 49, and citing Appx3389, ¶ 24 (in which ACQIS disputed only that a PCI bus transaction must be "converted into serial form at once")). Judge Burroughs explained that, therefore, "[a]t best, ACQIS asserts that EMC's products modify *some data* from a parallel to serial form prior to communicating or transacting that data, but ACQIS does not actually identify a *PCI bus transaction* that is converted from parallel to serial form and communicated by the accused products." *Id.* (citation omitted).

SUMMARY OF ARGUMENT

ACQIS raises two primary issues on appeal. First, ACQIS argues that a "PCI bus transaction" need not include everything required by the PCI Local Bus Specification for a PCI bus transaction. Second, ACQIS argues that the information communicated need not be converted from parallel to serial form. Because both

arguments are wrong, and it is undisputed that the accused devices do not practice the properly construed limitations of the asserted claims, this Court should affirm the judgment of non-infringement.

I. Both Judge Davis in Texas and Judge Burroughs in Massachusetts ruled that "a PCI bus transaction must include all information required by the PCI standard," Appx0507; Appx1702, and Judge Burroughs further confirmed that "the claims are limited by the [PCI Local Bus] Specification in its entirety," Appx0013. Both district courts (and the PTAB) rejected ACQIS's attempt to limit "PCI bus transaction" to a subset of the information required by the PCI standard—i.e., command, address, and data signals. ACQIS never sought reconsideration of this construction below, and does not even acknowledge on appeal the district courts' clear rulings that a PCI bus transaction must comply with the "entirety" of the PCI standard and include "all information" it requires for a PCI bus transaction. Appx0013; Appx0507; Appx1702. Instead, ACQIS feigns surprise at the district courts' construction, arguing that neither court really meant to require compliance with the entire PCI standard. On that basis, ACQIS contends that the district court erred by purportedly reinterpreting its construction at summary judgment and refusing to resolve a supposedly "new" claim construction dispute created by that reinterpretation.

Contrary to ACQIS's charge of procedural impropriety, the courts below had *twice* resolved the parties' dispute about the proper scope of "PCI bus transaction" before the summary judgment motion was filed. And both district courts consistently required the claimed "PCI bus transaction" to comply with ***the entirety*** of the PCI standard and include ***all information*** required by that standard. That requirement is correct: The specifications of the asserted patents make clear that signals other than command, address and data signals (e.g., control and parity signals) are part of a PCI bus transaction. The Local Bus Specification likewise demonstrates that control and parity signals are included in a PCI bus transaction—indeed, they are "fundamental" and "not optional," respectively. And although ACQIS now sings a different tune, ACQIS and its expert also admitted that a PCI bus transaction must include control and parity signals. The asserted patents and the PCI standard also require an address phase followed by one or more data phases.

This Court should confirm that a PCI bus transaction requires compliance with the entire PCI standard and includes all information it requires, and affirm the grant of summary judgment because the accused devices do not generate or communicate such a PCI-compliant bus transaction.

II. The accused products also do not convert a PCI bus transaction from parallel to serial form, as required by the district courts' construction of "encoded serial bit stream of [PCI] bus transaction" and related terms—even under ACQIS's

erroneous interpretation of the PCI bus transaction limitation. The district court recognized the parallel-to-serial requirement based not only on repeated clear and unmistakable disclaimers ACQIS made during the IPR proceedings, but also on the other intrinsic evidence, which clearly demonstrates that the PCI standard—a standard expressly incorporated into the claims—is parallel. A PCI bus transaction, therefore, must be converted from parallel to serial before being transmitted on the claimed serial channel.

ACQIS takes issue with the serialization construction, but cannot overcome its own disclaimers and the intrinsic evidence, which make clear that parallel-to-serial conversion is required. And, because ACQIS has not appealed the district court's finding that the accused products do not convert a PCI bus transaction from parallel to serial form, this Court should affirm the grant of summary judgement on this independent ground.[5]

ARGUMENT

I. Standard of Review

This Court reviews summary judgment decisions under the law of the regional circuit, here the First Circuit. *AntennaSys, Inc. v. AQYR Techs., Inc.*, 976 F.3d 1374, 1377 (Fed. Cir. 2020). The First Circuit reviews a district court's grant of summary

[5] There are additional reasons why EMC's products do not infringe the asserted patents, but EMC limits this brief to the issues ACQIS raises on appeal.

judgment de novo. *Murray v. Kindred Nursing Ctrs. W. LLC*, 789 F.3d 20, 25 (1st Cir. 2015). To prevail, "the moving party must show 'that there is no genuine dispute as to any material fact' and that it 'is entitled to judgment as a matter of law.'" *OneBeacon Am. Ins. Co. v. Com. Union Assur. Co. of Can.*, 684 F.3d 237, 241 (1st Cir. 2012) (quoting Fed. R. Civ. P. 56(a)). Where, as here, the moving party does not have the burden of proof at trial, it "can succeed on summary judgment by showing that there is an absence of evidence to support the nonmoving party's case." *Id.* (cleaned up). Accordingly, "a party opposing summary judgment must present definite, competent evidence to rebut the motion." *Torres v. E.I. Dupont De Nemours & Co.*, 219 F.3d 13, 18 (1st Cir. 2000) (cleaned up). "[M]ere existence of a scintilla of evidence is insufficient to defeat a properly supported motion for summary judgment." *Id.* (cleaned up).

This Court "review[s] a district court's claim constructions, including determinations of indefiniteness, de novo" and "review[s] subsidiary factual findings based on extrinsic evidence for clear error." *Synchronoss Techs., Inc. v. Dropbox, Inc.*, 987 F.3d 1358, 1365 (Fed. Cir. 2021).

II. The Accused Products Do Not Generate Or Communicate A PCI Bus Transaction In Accordance With The PCI Standard

Since the outset of this case, ACQIS has acknowledged that the claimed "PCI bus transaction" must be construed in accordance with the PCI Local Bus Specification, which provides a complete definition of what information comprises

a PCI bus transaction. *See* Appx0390–0391; Appx0507; *see also* Appx0391 (the invention "serialize[s] ***PCI standard signals specifically, not some generic signal or alternative***" (emphasis added)); Appx0395 ("'PCI bus transaction' merely refers to the ***information required by the PCI standard in order to create a PCI communication***" (emphasis added)); Appx1164 ("[R]eading the PCI Standard out of the claims would be wrong"). According to ACQIS, the asserted patents "adhere[] to the PCI standard," Appx0787; Appx0837, and "confirm[] that while the method of sending this information may change (from parallel to serial communication), ***the underlying transaction or information remains the same***," Appx0484 n.4 (citing the '873 patent at 20:27–47) (emphasis added).

This requirement makes sense: the purpose of ACQIS's invention was to bridge PCI-compliant devices with a new serial channel to improve communication speeds. By its nature, a PCI-compliant device expects—and is only capable of processing—transactions formatted according to the PCI standard. The claimed invention, therefore, converts a PCI bus transaction from its original parallel format into a serial format, transmits it over a serial bus, and reconstitutes it into the PCI format in toto, such that the PCI devices on either end are never aware that the transaction was ever serialized. That is why ACQIS argued that "adherence to the [PCI Local Bus Specification] ***is critical*** for interoperability with other components of a system" because "***[e]ven minor deviations from a standard will result in***

incompatible hardware and software." Appx0787 (emphasis added); Appx0836–0837. In other words, a "PCI bus transaction must comply with a particular format for peripheral devices and their PCI drivers to understand it." Appx0788; Appx0838. Thus, according to ACQIS, "do[ing] away with PCI" is "not the invention." Appx1031.

Yet, when faced with undisputed evidence that the accused products do not infringe because they do not generate PCI-compliant transactions, ACQIS argued on summary judgment, and repeats on appeal, that by claiming the PCI standard, it really meant to claim only a subset of that standard. But as its own expert explained unequivocally: "what is in the standard is what it is, no more no less." Appx0924 (150:19–21). ACQIS claimed the PCI standard and must live with it in its entirety.

A. Both District Courts Correctly Ruled That A "PCI Bus Transaction" Requires Compliance With The Entire PCI Standard

Consistent with the asserted patents' specifications and the PCI Local Bus Specification, both of which are part of the intrinsic record, the Texas and Massachusetts district courts agreed with the parties that a "PCI bus transaction" must adhere to the PCI standard. Both district courts also rejected ACQIS's attempt to limit that standard in order to create an infringement argument, and ruled that a "PCI bus transaction" "must include ***all information required by the PCI standard***" and comply with the PCI standard "***in its entirety***." Appx0507 (emphasis added);

Appx1702–04; Appx0013 (emphasis added). This aspect of the district courts' claim construction rulings is correct and should be affirmed.

ACQIS previously agreed that a PCI bus transaction must be in accordance with the PCI Local Bus Specification, which is very clear about the requirements for a PCI bus transaction—it is, after all, the document that explains how to comply with the PCI standard. But to preserve its strained infringement position, ACQIS now argues that it did not mean to include all aspects of the PCI standard in the asserted patents, comparing a PCI bus transaction to a simple telephone conversation. Br. 47–51. Unlike a telephone conversation (which may be transmitted in several different ways), however, a PCI bus transaction is defined by the PCI standard, and a standard does not tolerate deviation. *See* Appx3598 (126:13–21) (ACQIS's expert explaining that "if you violate parts of [the PCI standard] you don't have a standard anymore"). ACQIS's arguments, therefore, are contradicted by the very standard it claimed.

ACQIS attempts to evade the requirements of the PCI standard by parsing the PCI Local Bus Specification into "physical" and "transaction" layers, and redefining a PCI bus transaction based on its fabricated distinction between the two. But the PCI Local Bus Specification does not divide the PCI standard into layers (indeed, it does not even use the term "layer"), as EMC's expert explained to the district court. *See* Appx3282–3283. To the contrary, it specifies that all the required signals

constitute a PCI bus transaction—command, address, data, parity, and control signals, among others. *See* Appx2244–2248; Appx2262–2263; Appx2273–2275. In any event, as Judge Burroughs explained, prior to summary judgment, "ACQIS never attempted to parse the [PCI Local Bus] Specification in order to differentiate the elements that describe the methodology of the PCI bus transaction from those that describe the substance of the transaction," Appx0009, even though ACQIS had years and multiple chances in which to do so.

Because the PCI Local Bus Specification nowhere restricts a PCI bus transaction to only command, address, and data signals, every tribunal to consider ACQIS's attempts to limit a PCI bus transaction to only a subset of the PCI standard has correctly rejected it.

1. A PCI Bus Transaction Requires Control Signals

The PCI Local Bus Specification provides that control signals (like FRAME#, IRDY#, and TRDY#) control "[t]he ***fundamentals of all PCI data transfers***." Appx2262 (emphasis added). It further explains that the control signals delineate a PCI bus transaction by controlling when each phase of the transaction begins and ends. *See* Appx2246–2247; Appx2273–2275. Indeed, although ACQIS admits that a PCI bus transaction is defined by address and data phases, Br. 49, it fails to acknowledge that according to the PCI Local Bus Specification, each phase is in turn defined by these control signals, which must therefore be included in a PCI bus

transaction. The PCI Local Bus Specification also clearly separates control signals from command signals. *See, e.g.*, Appx2246–2248. Thus, the PCI Local Bus Specification makes clear that control signals are an integral part of a PCI bus transaction.

The specifications of the asserted patents also leave no doubt that a PCI bus transaction must include control signals, and also expressly distinguishes them from (the separately required) command signals. *See, e.g.*, Appx0153 ('873 patent, 20:44–47) (describing that "4 PCI C/BE# [3::0] signals" are transmitted separately from "PCI control signals, such as FRAME#, IRDY#, and TRDY#"); *id.* ('873 patent, 20:30–37) (describing that "in each clock cycle," "PCI command information" is sent separately from "control information"); Appx0135 ('873 patent, fig. 16) ("FRAME# . . . [i]ndicates beginning and duration of a PCI transaction"). And that makes sense, because the PCI standard requires *both* types of signals to be included in a PCI bus transaction.

ACQIS's statements in the IPRs also demonstrate that control signals are a required part of a PCI bus transaction. For example, ACQIS conceded that its invention "maintain[s] compatibility with [the PCI] standard" by "retaining PCI communication on the CPU side" so that "the system does not require new drivers or peripheral devices." Appx0790–0791. And during the IPR hearing, ACQIS confirmed that "if you look at the standard, ***there are three types of information***

included in every PCI transaction"—"[t]here's an address, there's data and ***then there's control***. That's straight out of the standard." Appx1032 (35:13–17) (emphasis added). ACQIS also argued that "[t]o carve control bits out . . . is to make sure [the PCI bus transaction] does not comply with either the standard of a PCI or the purpose of the invention." Appx1035 (38:15–17); *see also id.* (38:9–12) (ACQIS arguing that the claims require communicating "the information necessary to make ***a PCI transaction under the defined standard***," which "***includes the control bits every time***." (emphasis added)). ACQIS even stated that "[t]here is no such thing . . . as a PCI transaction that does not have control bits," and distinguished the Horst and Bogaerts prior art references on the basis that they do not disclose "transmitting any type of control bits." *Id.* (38:13–15).

Similarly, ACQIS's IPR expert, Dr. Lindenstruth, admitted that a PCI bus transaction must include all information required by the PCI Local Bus Specification, including control signals. For example, when asked whether "all of the elements of the PCI bus transaction have to be encoded [and communicated], including the address, data, ***control signals***, et cetera," ACQIS's expert answered "***[w]hatever pertains to the PCI transaction otherwise it wouldn't be complete***, yeah." Appx0943 (169:2–8). ACQIS's expert also testified that "control lines, such as frame, target[,] ready . . . . ***define the PCI transaction***. . . . ***So they would have to be—they define the transaction, so have to be there***." Appx0919–0920 (145:18–

146:17). Later in the deposition, ACQIS's expert again confirmed that "a PCI bus transaction . . . ***has to include everything necessary*** to define that transaction accurately," Appx0928 (154:4–8), and explained that "***what is in the standard is what it is, no more no less***," Appx0924 (150:19–21). ACQIS's district court expert, Dr. Gafford, similarly admitted in prior litigation that "an encoded PCI transaction is not just the data in the transaction, ***but all the PCI signals necessary for the data to be transferred using the PCI bus***"—i.e., control signals. Appx1745 (emphasis added); Appx1752; Appx1776.

Having overcome invalidity, ACQIS is now advancing a different construction in an effort to avoid the judgment of non-infringement. But this Court has "repeatedly rejected efforts to twist claims, 'like "a nose of wax,"' in 'one way to avoid [invalidity] and another to find infringement.'" *Data Engine Techs. LLC v. Google LLC*, 10 F.4th 1375, 1381 (Fed. Cir. 2021) (alteration in original). Recognizing that its admissions during the IPRs are fatal to its infringement case, ACQIS tries to explain them away by arguing that its counsel and expert were actually referring to *command* bits, not *control* bits. Br. 25–26, 58–60. But ACQIS never even explains its IPR expert's admissions, pointing only to post-hoc rationalization by its district court expert who testified well after the IPRs and the *Markman* proceedings in Massachusetts. *See* Br. 59 (citing Appx2601 (2018 expert report); Appx2158 (2018 deposition)). In any event, both of ACQIS's IPR

representatives were clear in their choice of words, and ACQIS makes no suggestion that either was acting beyond his respective competence or authority. More importantly, ACQIS did not seek to modify the intrinsic record it created before the PTAB, and is bound by that record in subsequent litigation. That is what a disclaimer *is*.[6]

In any event, ACQIS's argument is belied by the asserted patents and the PCI Local Bus Specification, which consistently and unequivocally separate command signals from control signals, thereby making clear that the terminology is not interchangeable. *See, e.g.*, Appx0146 ('873 patent, 5:31–44); Appx0153 ('873 patent, 20:30–37, 20:44–47); *cf.* Appx0152 ('873 patent, 17:28–32); *see also* Appx2246–2248, Appx2258–2262. And ACQIS itself previously distinguished these two types of signals. *See* Appx0837 ("The PCI standard bus was a 32-bit wide parallel bus with . . . separate command and timing control lines"); Appx0901 (same). ACQIS's post hoc attempts to rehabilitate its prior admissions are not believable when weighed against this intrinsic evidence and its own multiple

[6] Even if ACQIS's "repeated and consistent remarks" during the IPRs (which are part of the prosecution history) "'do not rise to the level of unmistakable disavowal, they do inform the claim construction'" and help "define [this] claim term." *Personalized Media Commc'ns, LLC v. Apple Inc.*, 952 F.3d 1336, 1345 (Fed. Cir. 2020) (quoting *Shire Dev., LLC v. Watson Pharms., Inc.*, 787 F.3d 1359, 1366 (Fed. Cir. 2015)).

statements to the contrary, and cannot explain away its clear admission that control signals are separately required to be included in a PCI bus transaction.

ACQIS also resurrects on appeal its failed argument from the district court that control signals cannot be part of a PCI bus transaction if no physical PCI bus is required. Br. 46–47. For example, ACQIS points to Figure 8 of the '415 patent[7] as describing an embodiment without a physical PCI bus, and contends that the district court's construction requiring control signals is "illogical" in view of this embodiment. Br. 47. But ACQIS never explains how control signals, which the PCI Local Bus Specification describes as "fundamental" to a PCI bus transaction and which the asserted patents repeatedly disclose, can be omitted without violating the PCI standard.

Moreover, Figure 8 (which in any event shows only a "partial block diagram," Appx0147 ('873 patent, 7:65–67)), *does* include a physical PCI bus on one side (the peripheral side), Appx0127—as does every other embodiment in the asserted patents. Even that embodiment, therefore, necessarily requires a complete PCI bus transaction—including control signals—to be reconstituted for transmission on that bus. ACQIS itself confirmed during the IPRs that "Figure 8 is a PCI limited embodiment," and "require[s] a PCI transaction to take place. . . [s]o all of [the] PCI-

[7] Presumably, ACQIS means Figure 8 of the '416 patent (which is identical to Figure 8 of the '873 patent), because there is no '415 patent among the asserted patents.

compliant drivers know how to read it." Appx1707–1708 (quoting Appx1042 (45:7–12); Appx1043 (46:14–21)). ACQIS further argued that although "the claims don't require a bus," "[y]ou could generate a PCI transaction without a bus" because "[y]ou are looking at the standard the whole time." Appx1043–1044 (46:14–47:1). In other words, the asserted patents (including Figure 8) describe a system that is necessarily compatible with the physical PCI architecture and includes all requirements of the PCI standard. The claimed system must allow for the presence of a physical PCI bus, and must therefore include all the information such a bus would require.

As Judge Burroughs correctly explained, "[a]lthough ACQIS argued strenuously and successfully that a PCI bus was not required in a PCI bus transaction, ACQIS never sought to disavow the elements of the [PCI Local Bus] Specification pertaining to a physical bus." Appx0009. And although Judge Burroughs "agree[d] with ACQIS that a PCI bus transaction does not require the presence of a PCI bus," she explained that she "cannot ignore that the PCI Local Bus Specification was developed for communication over a PCI bus." Appx1709. Thus, a PCI bus transaction cannot be "in accordance" with the PCI standard if it is missing portions that the PCI Local Bus Specification teaches are required for compliance with that standard.

Based on overwhelming intrinsic (and extrinsic) evidence, both district courts correctly ruled that a "PCI bus transaction" must include *all* information required by the PCI standard, including control signals. Appx0507; Appx1702. Judge Burroughs further correctly ruled based on this intrinsic record that "communicating . . . [a] PCI bus transaction" requires communicating all bits—including "control bits." Appx0012. Indeed, ACQIS agreed to the district court's construction requiring communication of all bits, including control bits, Appx1711–1712, and Judge Burroughs was correct to hold ACQIS to that agreement, *see Synchronoss*, 987 F.3d at 1368 (affirming grant of summary judgment after patentee agreed to a claim construction at the *Markman* hearing, and rejecting patentee's argument that the district court "misinterpreted" counsel's agreement). Concluding that "the claims are limited by the [PCI Local Bus] Specification in its entirety," Appx0012–0013, Judge Burroughs then applied these constructions to find that the accused products do not infringe. That ruling was entirely justified, because ACQIS put forth no evidence that the accused products functioned according to the PCI Local Bus Specification, as required by the district courts' constructions. Indeed, as the district court explained, "ACQIS d[id] not dispute that EMC's products do not include these features" required by the PCI standard.[8] Appx0008. This Court should

[8] ACQIS also moved for summary judgement of infringement, admitting that "the parties have no factual dispute regarding the structure, function, or operation of the accused . . . products." Memorandum in Support of Plaintiff

affirm the district court because all of ACQIS's challenges to the district courts' constructions contradict the PCI standard and accordingly must be rejected.

2. A PCI Bus Transaction Requires Parity Signals

The PCI Local Bus Specification also makes clear that parity signals are "not optional." Appx2247; Appx2332–2333. The asserted patents similarly demonstrate that parity signals are required, describing parity as a "primary bus PCI signal[]," Appx0154 ('873 patent, 22:28–31), that "is sent one cycle after address or data is valid," Appx0135 ('873 patent, fig. 16). This intrinsic evidence confirms that parity signals must also be included in a PCI bus transaction.

As with control signals, ACQIS attempts to escape the clear requirements of the PCI standard by referring to parity signals as "physical layer" signals and arguing that they cannot be part of a PCI bus transaction because the claims were construed to not require a physical PCI bus. Br. 33, 46–47. Even if so-called "physical layer" signals were excluded from the claim scope (and they are not, *see supra* at 30–36), parity signals have nothing to do with a physical bus. The PCI Local Bus Specification categorizes parity signals as part of the "Address and Data Pins" functional group, Appx2246–2247, and explains they are used for error detection, not control of a physical bus, Appx2332–2333. Thus, even if signals that control a

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ACQIS, LLC's Motion for Partial Summary Judgment of Direct Literal Infringement at 1, *ACQIS, LLC v. EMC Corp.*, No. 14-CV-13560-ADB (D. Mass. July 21, 2018), ECF No. 528.

physical bus were to be excluded, ACQIS has not explained how that could apply to parity signals.

ACQIS's efforts to exclude parity signals from a PCI bus transaction are also logically flawed. The PCI Local Bus Specification provides that one parity signal is sent after *each* address and data phase of a PCI bus transaction. Appx2332–2333. Excluding parity signals from a PCI bus transaction, as ACQIS seeks to do, would therefore make no sense, because each parity signal would then split a PCI bus transaction (which comprises both address and data phases) into pieces. Nothing in the PCI Local Bus Specification even suggests that a PCI bus transaction can be fragmented in this way.

ACQIS argues that excluding parity signals does not contradict the PCI standard because its expert purportedly confirmed that "parity signals are sent in a later phase." Br. 52. But ACQIS does not explain why that matters because any "later phase" would still be one of the address or data phases that constitute a PCI bus transaction. Moreover, the expert testimony ACQIS cites does not even mention parity. *See* Appx3397 (¶ 19). And even if it did as ACQIS pretends, the PCI Local Bus Specification contradicts that testimony, because it requires a parity signal to be sent after *each* address and data phase that *together* comprise a single PCI bus transaction. Appx2246–2247; *see Summit 6, LLC v. Samsung Elecs. Co.*, 802 F.3d 1283, 1290 (Fed. Cir. 2015) (explaining that expert testimony "may not be used 'to

contradict claim meaning that is unambiguous in light of the intrinsic evidence'" (quoting *Phillips v. AWH Corp.*, 415 F.3d 1303, 1324 (Fed. Cir. 2005) (en banc))). Because the intrinsic evidence clearly demonstrates that parity signals must be included in a PCI bus transaction, ACQIS's arguments to the contrary fail.

3. A PCI Bus Transaction Requires Phases

The PCI Local Bus Specification also requires that a PCI bus transaction consist of "[a]n address phase" followed by "one or more data phases." Appx2358. These phases are not signals; instead, each phase is a clock cycle (i.e., a period of time) in which certain signals (including command, address, data, and control signals) are sent. *See* Appx2273–2274 (illustrating phases in timing diagrams); Appx2358. Similarly, the asserted patents describe the phases (and associated clock cycles) of a PCI bus transaction. *See* Appx0135 ('873 patent, fig. 16); Appx0153 ('873 patent, 20:40–44) (describing address and data cycles). ACQIS and its expert repeatedly confirmed during the IPRs that the claims "require the address and data phases of a PCI bus transaction." Appx2090 (¶ 119); *see also, e.g.*, Appx0902; Appx3594 (114:14–115:14). By recognizing that the claims must comply with the entirety of the PCI standard, the district court therefore properly required a PCI bus transaction to have an address phase followed by one or more data phases. *See* Appx0008–0009. ACQIS recognizes this requirement on appeal by admitting that a PCI bus transaction is defined by address and data phases, Br. 49, yet its proposed

construction of "PCI bus transaction" improperly omits those phases by focusing only on "command, address, and data information," Br. 35. This is yet another reason why ACQIS's proposed construction violates the PCI standard and should be rejected.

In sum, because the asserted patents require compliance with the entirety of the PCI standard, the district courts correctly construed "PCI bus transaction" to include all requirements of that standard. That construction should be affirmed. At the very least, ACQIS repeated statements during the IPRs demonstrate that a PCI bus transaction must include control signals and phases as required by the PCI Local Bus Specification. *See supra* at 31–36, 40.

B. ACQIS Misrepresents The Proceedings Below

ACQIS erroneously asserts that neither district court explained "what information a 'PCI bus transaction' must include to be 'in accordance with the [PCI Local Bus Specification].'" Br. 23; *see also* Br. 19. ACQIS argues that both district courts actually meant to require compliance with only a portion of the PCI standard, but that Judge Burroughs supposedly reinterpreted at summary judgment the district courts' construction to require control and parity signals. Br. 33, 44–53. That is demonstrably false.

Both Judge Davis and Judge Burroughs could not have been clearer as to what information a PCI bus transaction must include—"***all information required by the***

PCI standard." Appx0507 (emphasis added); Appx1702. And Judge Burroughs further confirmed that a PCI bus transaction must comply with the PCI standard "in its entirety." Appx0013. Indeed, Judge Burroughs explained that Judge Davis's construction formed the basis for her summary judgment decision that the accused products could not infringe because they do not comply with the entire PCI standard. *See* Appx0008–0009. And Judge Burroughs expressly criticized ACQIS for its "attempts to skirt ***the claim construction set forth by Judge Davis and this Court.***" Appx0008 (emphasis added).

ACQIS never acknowledges these rulings in its opening brief. Yet, they show that the district courts were entirely consistent in construing "PCI bus transaction"—contrary to ACQIS's unsupported assertion that the rug was somehow pulled out from under it at the summary-judgment stage. ACQIS also does not acknowledge on appeal that it failed to seek reconsideration of Judge Davis's construction, arguing instead that there was no reason to disturb it. Appx1147; *see also* Appx1156; Appx1164. In other words, the only one reinterpreting the record here is ACQIS. Both district courts consistently (and correctly) required a PCI bus transaction to comply with the entire PCI standard, and ACQIS's argument that the district court somehow "misinterpreted its earlier claim construction of 'PCI bus transaction,'" Br. 33, is therefore pure fiction.

ACQIS also argues that the district court improperly barred its claim construction arguments at summary judgment as untimely, and that the district court was required to resolve all claim construction disputes prior to trial. Br. 34–44. But this argument is predicated on the false premise that EMC's summary judgment arguments were based on a claim construction position not previously addressed by the district court and to which ACQIS could not have previously responded. *See, e.g.*, Br. 38. ACQIS even blames EMC for not objecting to its "repeated statements" that a PCI bus transaction is limited to only command, address, and data signals, pretending that it was somehow surprised by EMC's non-infringement arguments at summary judgment. Br. 37. ACQIS claims that it "argued for years" that a PCI bus transaction was limited to only a subset of the PCI standard, Br. 35–36, but omits the critical fact that the district courts also consistently *rejected* that argument for years. There was no "new" claim construction dispute here—as demonstrated above, EMC moved for summary judgment based on the claim construction that governed the case since Judge Davis explained in 2015 that a PCI bus transaction included "all information required by the PCI standard," Appx0507, and Judge Burroughs confirmed the same in 2017, Appx1702. If ACQIS chose to ignore the district courts' clear orders, the fault lies with ACQIS.

ACQIS invokes *O2 Micro International Ltd. v. Beyond Innovation Technology Co.*, 521 F.3d 1351 (Fed. Cir. 2008), for the well-settled proposition that

a district court must resolve a fundamental claim construction dispute. With respect to the principal issue on appeal, however, the district courts ***did so twice***, each time rejecting attempts by ACQIS to limit a "PCI bus transaction" to "command, address, and data signals." On that basis, Judge Burroughs recognized that "ACQIS's arguments are attempts to skirt the claim construction set forth by Judge Davis and this Court," Appx0008, and found ACQIS's arguments on summary judgment to be untimely, Appx0009–0010. That conclusion was entirely proper—*O2 Micro* does not require a district court to repeatedly decide a dispute already resolved or continuously rehear the same arguments that it already rejected. "Claim construction is not an obligatory exercise in redundancy" but is instead "a matter of resolution of disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims." *O2 Micro*, 521 F.3d at 1362 (cleaned up). A district court need only "define[] the claim with whatever specificity and precision is warranted by the language of the claim and the evidence bearing on the proper construction." *Eon Corp. IP Holdings v. Silver Spring Networks*, 815 F.3d 1314, 1319 (Fed. Cir. 2016) (citation omitted). The district courts here twice clarified and explained the scope of "PCI bus transaction" covered by the asserted patents, and Judge Burroughs was therefore correct, on this record, to reject any further attempts by ACQIS to reargue this construction.

C. ACQIS' Arguments Regarding Address And Data Claims Are Irrelevant And Wrong

1. ACQIS asserts (Br. 29) that the district court never reached its "separate arguments" concerning the address and data claims, such as, for example, claim 61 of the '873 patent, which recites that "the encoded serial bit stream of [a] PCI bus transaction comprises encoded *PCI address and data bits.*" Appx0165 ('873 patent, 44:5–7) (emphasis added). But ACQIS never asked the district courts to treat these claims differently for purposes of claim construction or infringement. Rather, ACQIS has always treated all asserted claims the same vis-à-vis the "PCI bus transaction" limitation, which makes sense because all of the asserted claims require a complete PCI bus transaction. ACQIS's argument is therefore forfeited.

ACQIS argues on appeal that it explained to Judge Burroughs that, "even if a [PCI bus] 'transaction' requires [control bits], summary judgment would still be inappropriate against the Address and Data Claims, which explicitly recite transmitting only the 'address and data bits of a PCI bus transaction.'" Br. 27 (quoting Appx3337–3338). But in fact ACQIS *never* made this argument on summary judgment or at any other time before the district courts. Instead, ACQIS only pointed to the so-called "address and data claims" as examples where the claims "state precisely what must be communicated" as part of its argument that the asserted claims *taken together* do not require "encoding, serializing, and communicating" control signals or bits. Appx3337. ACQIS never argued that the "address and data"

claims should be construed separately to exclude everything but the address and data signals/bits from a PCI bus transaction. ACQIS likewise treated all of the challenged claims the same during the IPR proceedings. *See, e.g.*, Appx0800–0802 (treating all challenged claims of the '873 patent together and arguing that Horst does not teach "the system claimed in claim 54 or any of its dependent claims, including claims 56-61," because "Horst teaches a different architecture and never serializes an actual PCI bus transaction").

ACQIS's focus always remained on whether all of the asserted claims included control signals as part of a PCI bus transaction, and the district courts correctly rejected that argument. The first time that ACQIS raised the argument that address and data claims should be treated separately for claim construction or infringement purposes is on appeal, and consequently, that argument is waived. *See Conoco, Inc. v. Energy & Env't Int'l, L.C.*, 460 F.3d 1349, 1358–59 (Fed. Cir. 2006) ("[A] party may not introduce new claim construction arguments on appeal or alter the scope of the claim construction positions it took below").

2. ACQIS's arguments based on the "address and data" claims are misplaced because intrinsic and extrinsic evidence confirms that those claims still require a complete PCI bus transaction—i.e., all information required by the PCI Local Bus Specification. The "address and data" claims generally recite that a "***PCI bus transaction comprises*** encoded PCI address and data bits." Appx0165 ('873 patent,

44:5–7) (emphasis added); *see also* Appx0246 ('814 patent, 28:34–39) (reciting communicating "address and data bits ***of [a] PCI bus transaction***" (emphasis added)). Critically, this claim language demonstrates that a complete PCI bus transaction must exist. An analogy is helpful to illustrate why these claims still require a full PCI bus transaction to be generated: to give someone a piece of pie, that piece must come from a previously baked whole pie. In other words, a piece of pie cannot exist without there first being a whole pie. Likewise, address and data bits "***of*** [a] PCI bus transaction" cannot exist or be communicated without there first being a complete PCI bus transaction. Moreover, these claims do not foreclose the existence of a full PCI bus transaction. *See CIAS, Inc. v. All. Gaming Corp.*, 504 F.3d 1356, 1360–61 (Fed. Cir. 2007) (noting the "long-standing recognition" that "comprising" and "comprises" are "open-ended term[s]" that "'do[] not exclude additional, unrecited elements'" (citation omitted)). Indeed, ACQIS has pointed to no support in the asserted patents (because there is none) that the address and data bits can be generated out of thin air without a full PCI bus transaction. And there is not a single embodiment described in the asserted patents' specifications where only address and data bits are sent; each embodiment transmits other information required by the PCI Local Bus Specification. *See, e.g.*, Appx0153 ('873 patent, 20:27–60).

In addition to the clear intrinsic evidence, ACQIS's expert also agreed that although the claims recite "address and data bits," they still require all of the

information specified by the PCI standard because that information must be recreated on the receiving end after transmission in order for the PCI-compliant devices to understand it. Appx0928–0929 (154:21–155:18) ("confirm[ing]" that communicating address and data bits of PCI bus transaction in serial form (as recited in claim 24 of the '814 patent) "requires that what is communicated are all of the pieces of information needed to recreate the PCI bus transaction on the other end of the serial transmission").

ACQIS also confirmed during the *Markman* hearing in Massachusetts that a pre-existing full PCI bus transaction (including control bits) is required for *all* claims, including the address and data claims. Indeed, the address and data claims, properly understood, do not limit the information that is communicated, but instead limit the specific PCI bus transactions covered by these claims.[9] Specifically, ACQIS explained that the only reason these claims expressly recite "address and data bits" is to distinguish between communicating different *types* of PCI bus transactions (i.e., those that require a valid address and those that do not). The address and data claims cover only PCI bus transactions with valid addresses. *See* Appx1634 ("[T]he claim specifically culls out address and data bits of the

[9] EMC takes no position at this time as to whether the address and data claims also require transmission of the control and parity bits that are part of the PCI bus transaction, because resolution of this question is unnecessary for the present appeal.

transaction. . . . ***[to] distinguish[] [it] from transactions . . . that don't have a valid address***." (emphasis added)); Appx1637 (arguing that unlike claims that do not require a valid address, inclusion of the "address and data bits" language is to indicate that a claim "that requires the transmission of an address[] is more limited to the other transactions like memory read, memory write and things like that. This is again explaining ***the types of transactions*** that would be included within the configuration." (emphasis added)); Appx1637 ("[W]hat's required by [the address and data claims] when read in light of the specification is that the information ***actually communicated*** over the serial channels includes address and data bits ***of a PCI standard bus transaction***." (emphasis added)). Thus, contrary to its arguments on appeal, ACQIS confirmed to Judge Burroughs that *all* asserted claims still require generating a full PCI bus transaction (including control bits).

Consistent with the intrinsic evidence and ACQIS's arguments and expert testimony, a PCI bus transaction is required by all asserted claims, and—as both district courts concluded—such a transaction must include all information required by the PCI standard, including control and parity signals. Because the accused products do not include all of the information comprising a PCI bus transaction, do not communicate all required bits of a PCI bus transaction, and do not communicate information in separate address and data phases, the district court's grant of summary judgment should be affirmed.

III. The Accused Products Do Not Serialize A Parallel PCI Bus Transaction

Even if ACQIS were correct that a PCI bus transaction need not comply with the entire PCI standard, the district court's summary judgment order is supported by a second and independent ground—that the accused products do not "serialize" a PCI bus transaction from parallel form. On appeal, ACQIS challenges only the district court's construction requiring "conversion" (or "serialization") from parallel to serial form, Br. 62–68, and does not dispute that the accused products do not infringe under that construction. Because the district court's construction is correct and ACQIS has waived its infringement argument under that construction, this Court could affirm the order below on this alternate ground.

A. ACQIS's Challenges To The Construction Of "Encoded Serial Bit Stream Of [PCI] Bus Transaction" Are Meritless

As the district court recognized, "ACQIS's ***numerous and repetitive statements in the IPRs*** clearly and unmistakably show" that encoding a PCI bus transaction requires conversion "for serial transmission from a parallel form." Appx1708. ACQIS's efforts to avoid the consequences of its own statements to the PTAB are unavailing. The Massachusetts district court included in its *Markman* order three-and-a-half pages of quotations from the IPR proceedings where ACQIS disclaimed anything other than parallel-to-serial conversion. Appx1705–1708.

For example, as Judge Burroughs explained, ACQIS stated in its Patent Owner Responses that "one ***key*** to the invention was to ***serialize the otherwise***

parallel PCI bus transactions to increase communication speeds for peripherals." Appx0782 (emphasis added); Appx0831 (same). Similarly, ACQIS argued that its invention improves communication "by making the PCI communication ***serial rather than parallel***." Appx0786 (emphasis added); Appx0836 (same). ACQIS also explained that "[t]he trick [to the claimed inventions] was ***to use the existing PCI standard*** and make it faster for communicating with peripheral devices." Appx0790 (emphasis added); Appx0840 (same). ACQIS then admitted that "[t]he PCI standard"—to which it assured the Board the asserted patents adhere—"specified 32-bit ***parallel*** communications." Appx0789 (emphasis added); Appx0839 (same). On this basis, ACQIS even distinguished prior art by claiming that "[these references] ***never used a serialized*** PCI bus transaction, ***only parallel***." Appx0783 (emphasis added); Appx0832 (same).

ACQIS's expert also agreed that parallel-to-serial conversion of a PCI bus transaction is required by the claims: When asked whether "the claims . . . contemplate some sort of ***transformation of the PCI bus transaction into a format that is serially transmitted*** and then, on the other end, it would be converted back into PCI bus transaction format," the expert answered "in the context of the patent[,] . . . ***yes***." Appx0923–0924 (149:20–150:5) (emphasis added).

ACQIS continued to emphasize the importance of parallel-to-serial conversion to the claimed invention throughout the IPR hearing. For example,

ACQIS stated that "***the whole point***" of the claimed invention was "***I'm going from parallel, I'm putting on a serial line.***" Appx1027 (emphasis added). ACQIS doubled down on this argument later in the hearing, asserting that "[a]ll of the computers out there have PCI. And so the point was, how do you speed up PCI? ***And the point is you take it from parallel to serial and then back to parallel***." Appx1031 (emphasis added). It would be difficult to find a disclaimer that is clearer or more unmistakable than ACQIS's statements.

ACQIS argues that the district court took those quotes out of context, Br. 66, but that is not so. ACQIS repeatedly argued that parallel-to-serial conversion was "key" to the invention, and EMC took ACQIS at its word. Appx1524; *see Tech. Props. Ltd. v. Huawei Techs. Co.*, 849 F.3d 1349, 1357 (Fed. Cir. 2017) ("Prosecution disclaimer can arise from . . . arguments"). ACQIS now claims that it only made those statements to emphasize that the prior art did not disclose a PCI-compliant address. Br. 66. But this post hoc rationalization does not alter ACQIS's emphatic, repeated assertions that parallel-to-serial conversion is "the whole point" of the claimed inventions. Appx1027; *see SpeedTrack, Inc. v. Amazon.com, Inc.*, 998 F.3d 1373, 1380 (Fed. Cir. 2021) (prosecution disclaimer may be found "even if the applicant distinguishes the reference on other grounds as well"); *X2Y Attenuators, LLC v. ITC*, 757 F.3d 1358, 1362 (Fed. Cir. 2014) (finding disclaimer where an element was described as "essential" and "universal" to the invention).

ACQIS also argues no disclaimer occurred because it proposed a construction during the IPRs that included types of encoding that "have no relationship to parallel signals." Br. 63. But as Judge Burroughs correctly explained, that argument fails because the types of encoding on which ACQIS relies ("group[ing] bits into a specified size block" and "order[ing] bits onto one or more serial transmission lines") also involve parallel-to-serial conversion. *See* Appx0152 ('873 patent, 17:54−60); *see also* Appx1710 n.4.[10]

ACQIS also attempts to distance itself from its IPR disclaimers by arguing that it never distinguished the prior art based on the parallel-to-serial conversion requirement. Br. 64. That misrepresents the record. In fact, ACQIS repeatedly argued that PCI bus transactions in the prior art "are never serialized." Appx0780; *see also* Appx0783 ("Horst never used a serialized PCI bus transaction, only parallel"); Appx0800–0801 ("Horst creates a parallel (not serial) PCI bus transaction" which is "never serialize[d]"); Appx1043 ("Horst doesn't have a PCI transaction that is then serialized"). These arguments further emphasize ACQIS's disavowal.

Moreover, the district court did not rely solely on its disclaimer finding. Judge Burroughs also explained that the asserted patents' specifications independently

[10] The district court cited page 17 of ACQIS's brief (Appx1172), but the relevant argument appears on page 19 of the brief (Appx1174).

demonstrate the parallel-to-serial conversion requirement. Appx1709–1710. Specifically, Judge Burroughs pointed out that the '873 patent specification describes "multiplexed ***parallel*** address/data (A/D) bits and control bits." Appx1709 (citing Appx0152 ('873 patent, 17:41–43)) (emphasis added). The specification further states that "[t]he multiplexed ***parallel*** A/D bits and some control bits input to [a] transmitter 1030 are ***serialized by parallel to serial converters*** 1032 [and 1033] into 10 bit packets." Appx0152 ('873 patent, 17:54–60) (emphasis added); *see also* Appx1710 n.4. Judge Burroughs also explained that "a detailed diagram of one embodiment of the host interface controller shows that it has a 'parallel to serial converter' and '[e]ncoders' that 'format the PCI address/data bits to a form more suitable for parallel to serial conversion." Appx1710 (citing Appx0129 ('873 patent, fig. 10); Appx0151 ('873 patent, 16:55–58)) (alteration in original). The consistency between the asserted patents' specifications and ACQIS's repeated statements during the IPRs supports a finding of disavowal. *See Traxcell Techs., LLC v. Nokia Sols. & Networks Oy*, 15 F.4th 1136, 1144–45 (Fed. Cir. 2021).

Reading the claims and the specification of the asserted patents in view of the PCI Local Bus Specification supports the parallel-to-serial conversion requirement. The district court explained that this term "essentially contains the following elements: (1) encoded, (2) serialized or 'serial bit stream,' and (3) PCI bus transaction." Appx1709. The district court then noted with disapproval that

"ACQIS focuses solely on the meaning of 'encoded,'" explaining that it "must interpret the term as a whole and in context with surrounding words." *Id.* ACQIS makes the same mistake on appeal, arguing that the district court erred by "conflat[ing] 'serialized' with conversion 'from a parallel form,'" because a serialized transaction need not start as parallel signals, but "can also be created from data in memory." Br. 67. ACQIS again ignores the context of the claim language—ACQIS focuses on the word "encoded," but ignores the third element of the term: the requirement that what is being serialized is a *PCI bus transaction*, not random "data in memory." As Judge Burroughs correctly explained and the PCI Local Bus Specification confirms, even if "a PCI bus transaction does not require the presence of a PCI bus," the PCI standard "was developed for communication over a PCI bus, which is indisputably parallel." Appx1709. Thus, reading this term in the context of the claim language, Judge Burroughs correctly concluded that "serializing a PCI bus transaction" requires conversion from parallel to serial. Appx1709–1710.

B. The Serialization Construction Is Dispositive

1. ACQIS inexplicably asserts that the district court's construction of "encoded serial bit stream of [PCI] bus transaction" is "non-dispositive." Br. 68. ACQIS is wrong.

Contrary to ACQIS's argument, the district granted summary judgment on the independent ground of its construction requiring parallel-to-serial conversion.

Appx0011. Judge Burroughs explained that ACQIS did "not dispute" that the asserted claims require a PCI bus transaction "beginning in parallel form, to be converted into serial form" and ruled that ACQIS failed to show that "EMC's accused products serialize a PCI bus transaction from a parallel form consistent with the asserted claims" and the district court's construction. Appx0012.

In this Court, ACQIS disputes the construction requiring "conversion" (or "serialization") from parallel to serial form, but does not dispute that under that construction, the accused products do not infringe. ACQIS is mistaken, therefore, that this issue is non-dispositive: Because the district court's construction is correct (as demonstrated above), it provides an independent, or alternative, ground for affirming the judgment of non-infringement. *See Acceleration Bay LLC v. 2K Sports, Inc.*, 15 F.4th 1069, 1076 (Fed. Cir. 2021) (holding an appeal moot because appellant "has forfeited any challenge to the district court's grant of summary judgment of non-infringement" by challenging only one of two independent grounds underlying the district court's order).[11]

Although it bore the burden to prove infringement, *see Medtronic, Inc. v. Mirowski Fam. Ventures, LLC*, 571 U.S. 191, 198 (2014), ACQIS failed to present

[11] Of course, ACQIS may not in its reply brief raise any challenges that it chose not to include in its opening brief. *See SmithKline Beecham Corp. v. Apotex Corp.*, 439 F.3d 1312, 1319 (Fed. Cir. 2006) ("Our law is well established that arguments not raised in the opening brief are waived").

evidence that the accused products serialize a PCI bus transaction (however construed) or raise any genuine issue of material fact on this point. Indeed, ACQIS's expert admitted that he did not know "whether the accused products first create a PCI bus transaction in parallel form and then convert that into serial form," as required by the district court's construction. Appx1758 (quoting Appx2185 (527:1–7)). He also could not identify any transaction in the accused products in parallel form that is serialized, as EMC explained. Appx1758–1759. That is because none exists.

Moreover, ACQIS presented no evidence that the accused products convert a "PCI bus transaction" from parallel to serial form even under its *own* truncated and thrice-rejected construction of that term (i.e., a transaction that includes only command, address, and data bits). Nor could it, because the accused products *never* generate at least a 32-bit address or data (as required by the PCI Local Bus Specification) in parallel format (or any format), let alone convert that address to serial form. As EMC explained on summary judgment, "[t]he only data that enters the parallel-to-serial converters [in the accused products] is a 10-bit symbol, encoded from a *single byte* of a PCI Express packet," and 10 bits cannot transmit 32 bits of address information as required by the PCI standard—and even as required by ACQIS's narrow construction of "PCI bus transaction." Appx1761–1762. ACQIS never plausibly disputed this fact. *See* Appx3367–3368 (conceding that the asserted

patents and the PCI Local Bus Specification convert parallel address and data information "32 bits at a time").

Therefore, the district court ruled on summary judgment that the accused products do not infringe. Judge Burroughs explained that even if "EMC's products modify *some data* from a parallel to serial form prior to communicating or transacting that data, . . . ACQIS does not actually identify a *PCI bus transaction* that is converted from parallel to serial form and communicated by the accused products." Appx0012. If the construction requiring parallel-to-serial conversion is sustained (as it should be), the judgment of non-infringement must be affirmed. *See OneBeacon*, 684 F.3d at 241 (summary judgment is appropriate where the movant does not bear the burden of proof and shows "that there is an absence of evidence to support the nonmoving party's case").

2. On appeal, ACQIS makes three additional arguments. Each is wrong.

First, ACQIS argues that because the term "encoded serial bit stream of [PCI] bus transaction" includes the phrase "PCI bus transaction," reversal of the district court's construction as to that latter phrase would require reversal in toto. Br. 55–56. That is wrong, because the accused products do not serialize a PCI bus transaction even under ACQIS's erroneous reinterpretation of the construction of that term, as explained above. Thus, even if "PCI bus transaction" were construed according to ACQIS's proposal, to require transmission of only some of the

information in the PCI standard, the accused products would still not meet that serialization limitation.

Second, ACQIS argues that the district court did not "rely" on its serialization construction to grant summary judgment. Br. 68. This argument blinks reality: The district court devoted an entire section of its opinion to this point, explained that the asserted claims require both a standard-compliant PCI bus transaction *and* serialization from parallel to serial form, Appx0011, and squarely ruled that EMC is entitled to a judgment of non-infringement because the accused products do not practice the serialization limitation, Appx0012–0013. As explained above, the district court found that at best, ACQIS argued that the accused products serialized "*some data*," Appx0012, but that data is not a serialized PCI bus transaction under any construction of that term.

Third, ACQIS asserts that it presented an "alternative infringement theory" in the district court. Br. 68. That is false: ACQIS never demonstrated parallel-to-serial conversion of a PCI bus transaction under any construction of that term. Even if it had, the district court did not accept (or rely on) any such theory, and ACQIS has not pressed on appeal any assignment of error in this respect. Accordingly, ACQIS has forfeited any argument for reversal based on its supposed alternative theory. *See SmithKline*, 439 F.3d at 1319.

ACQIS had the burden of coming forward with evidence that the accused products practice parallel-to-serial conversion under the court's construction of the "encoded serial bit stream of [PCI] bus transaction" limitation and related terms. It failed to do that. Therefore if the construction is sustained, as it should be, the summary judgment of non-infringement must be affirmed on this independent ground. *See Acceleration Bay*, 15 F.4th at 1076.

CONCLUSION

The judgment of non-infringement should be affirmed.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that on November 19, 2021, I served a copy of the foregoing brief on all counsel of record via the CM/ECF system.

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CERTIFICATE OF COMPLIANCE

1. This brief complies with the type-volume limitation of Federal Circuit Rule 32(b)(1) because it contains 13,916 words, excluding the parts of the brief exempted by Federal Circuit Rule 32(b)(2) and Federal Rule of Appellate Procedure 32(f).

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